

EXHIBIT C

We claim:

1. An intermediate product in the fabrication of a MOSFET, comprising:

a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift

5 layer having a plurality of source regions formed adjacent an upper surface thereof;

a first oxide layer on said upper surface of said drift layer;

a plurality of polysilicon gates above said first oxide layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions;

10 an oxide layer over said first source region of greater thickness than said first oxide layer; and,

an oxide layer over said first gate of substantially greater thickness than said oxide layer over said first source region.

2. A silicon carbide power MOSFET, comprising:

15 a silicon carbide wafer having a substrate and a drift layer on said substrate, said drift layer having a plurality of source regions formed adjacent an upper surface thereof;

a plurality of polysilicon gates above said drift layer, said plurality of polysilicon gates including a first gate adjacent a first of said source regions, said first gate having a top surface, a lower surface and a sidewall, said sidewall overlying said first source region;

20 a first oxide layer between said first gate lower surface and said upper surface of said drift layer;

a second, thicker oxide layer over said top surface and sidewall of said first gate; and,

a conformal layer of metal extending laterally across said first gate top surface and sidewall and said adjacent first source region.

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3. A method of fabricating a silicon carbide power MOSFET, comprising:

forming a source region adjacent an upper surface of a drift layer on a silicon carbide substrate;

30 oxidizing the silicon carbide to form a first oxide layer on said upper surface of said drift layer;

forming a polysilicon gate on said first oxide layer;

oxidizing said polysilicon gate and the silicon carbide adjacent thereto to form a second oxide layer having a substantially greater thickness over said gate than over the silicon carbide adjacent thereto;

5 etching said first and second oxide layers without a photomask over either layer, said etching substantially completely removing the oxide over the silicon carbide adjacent said gate while leaving a portion of said second oxide layer over said gate; and,

depositing metal over said gate and said adjacent source region without using a photomask to limit the lateral extent of the metal deposition across said gate and source

10 region.